Fpga Interview Questions And Answers

FPGA Engineer at a global technology-based trading firm - FPGA Engineer at a global technology-based trading firm 1 minute, 28 seconds - Find out what being an **FPGA**, Engineer is really like. Watch Maurice Daverveldt, an **FPGA**, Engineer at Optiver explain what it is ... 97ba4acbee What is metastability, how is it prevented? 97ba4acbee Q3: How do you design reliable synchronous RTL? 97ba4acbee Basic Embedded Hardware Interview Questions Part 1 FPGA - Basic Embedded Hardware Interview Questions Part 1 FPGA 53 seconds - Embedded Electronics Hardware Design Engineer **interview questions**, : **FPGA**,. 97ba4acbee What is a Shift Register? 97ba4acbee Question 19: What is false path? 97ba4acbee Q19: How would you diagnose an FPGA design that fails its throughput target? 97ba4acbee Question 9: What is RTL design? 97ba4acbee Name some Latches 97ba4acbee Question 17: What are setup and hold time violations? 97ba4acbee Question 25: What is IR drop? 97ba4acbee Q6 How many multiplexers can be implemented in one slice 97ba4acbee Question 8: What is CDC (Clock Domain Crossing) and how do you handle it? 97ba4acbee Question 13: What is DSP block and why do modern FPGAs include them? 97ba4acbee Keyboard shortcuts 97ba4acbee What is a FIFO? 97ba4acbee What should you be concerned about when crossing clock domains? 97ba4acbee Describe differences between SRAM and DRAM 97ba4acbee Question 4: What is timing closure and why is it important? 97ba4acbee Subtitles and closed captions 97ba4acbee Example Interview Questions for a job in FPGA, VHDL, Verilog - Example Interview Questions for a job in FPGA, VHDL, Verilog 20 minutes - NEW! Buy my book, the best **FPGA**, book for beginners: https://nandland.com/book-getting-started-with-**fpga**,/ How to get a job as a ... 97ba4acbee Question 15: What is HLS (High-Level Synthesis)? 97ba4acbee Intro 97ba4acbee Melee vs. Moore Machine? 97ba4acbee What is the purpose of Synthesis tools? 97ba4acbee Describe Setup and Hold time, and what happens if they are violated? 97ba4acbee Tel me about projects you've worked on! 97ba4acbee Name some Flip-Flops 97ba4acbee Question 18: What is multi-cycle path? 97ba4acbee Q10: How do you implement fixed-point arithmetic and prevent overflow in an FPGA? 97ba4acbee Spherical Videos 97ba4acbee Q9 How many luts are required for implementation of 2x21 97ba4acbee Q15: What is the difference between synthesis and place-and-route, and what reports do you inspect? 97ba4acbee Why might you choose to use an FPGA? 97ba4acbee Question 22: What is scan chain in VLSI? 97ba4acbee Question 7: What is the difference between synchronous and asynchronous resets? 97ba4acbee Like \u0026 Share 97ba4acbee Q18: How would you bring up and debug an FPGA design on a new board? 97ba4acbee Introduction 97ba4acbee Q2 How many LUTs 97ba4acbee Q16: What is partial reconfiguration, and what design challenges does it introduce? 97ba4acbee Crossing Clock Domains in an FPGA - Crossing Clock Domains in an FPGA 16 minutes - NEW! Buy my book, the best **FPGA**, book for beginners: https://nandland.com/book-getting-started-with-**fpga**,/ How to go from slow ... 97ba4acbee HWN - Real \"SoC Design Engineer - Digital\" Interview Questions - HWN - Real \"SoC Design Engineer - Digital\" Interview Questions 10 minutes, 8 seconds - We polled our Reddit community and you decided what content you wanted next! The team reached out to a seasoned Digital ... 97ba4acbee FPGA Design Engineer Interview Questions - FPGA Design Engineer Interview Questions 1 minute, 10 seconds - Interview Questions, for **FPGA**, Design Engineer.What are your professional objectives for an **FPGA**, Design Engineer?Tell me ... 97ba4acbee Question 12: Explain pipeline and its benefits in FPGA design. 97ba4acbee What is a UART and where might you find one? 97ba4acbee Q5 How many LUTs will be used 97ba4acbee Question 5: What is clock skew and how is it minimized? 97ba4acbee What is a Block RAM? 97ba4acbee FPGA Interview Questions and Answers Part 4 - FPGA Interview Questions and Answers Part 4 22 minutes - In this video, most commonly asked **FPGA**,/Emulation **interview questions**, are discussed with a good amount of explanation as well ... 97ba4acbee FPGA Engineer Interview Questions \u0026 Answers - FPGA Engineer Interview Questions \u0026 Answers 20 minutes - Are you preparing for an **FPGA**, Engineer **interview**,? In this video, we cover 20 essential **questions**, you're likely to encounter, ... 97ba4acbee Question 24: What is clock gating? 97ba4acbee Describe the differences between Flip-Flop and a Latch 97ba4acbee Inference vs. Instantiation 97ba4acbee Q4: What causes setup and hold violations, and how would you fix them? 97ba4acbee Q8 How many multiplexers are required for implementation of 16x21 97ba4acbee Q9: How would you design a robust finite-state machine in synthesizable RTL? 97ba4acbee Search filters 97ba4acbee Question 2: What is LUT and how does it work inside an FPGA? 97ba4acbee Q11: How would you design a high-throughput FIFO using FPGA block RAM? 97ba4acbee How is a For-loop in VHDL/Verilog different than C? 97ba4acbee Q12: What timing constraints are essential in an FPGA project, and how can bad constraints hurt? 97ba4acbee Question 16: What is the difference between blocking and non-blocking assignments in Verilog? 97ba4acbee Question 20: What is a latch, and why is it often avoided? 97ba4acbee Question 11: What is floorplanning in FPGA design? 97ba4acbee Q8: What are the benefits and costs of pipelining an FPGA datapath? 97ba4acbee Question 21: Explain power optimization techniques in FPGA/VLSI. 97ba4acbee Q14: When would you use formal verification instead of simulation for FPGA RTL? 97ba4acbee Q20: How would you explain a challenging FPGA project or debugging incident in an interview? 97ba4acbee Q4 How many 4x1 multiplexers 97ba4acbee Q5: How do you approach timing closure on a difficult FPGA design? 97ba4acbee Synchronous vs. Asynchronous logic? 97ba4acbee Q10 Why to answer this question 97ba4acbee What is a DSP tile? 97ba4acbee FPGA Interview Advanced Questions \u0026 Answers (2026) for Experienced Engineers - FPGA Interview Advanced Questions \u0026 Answers (2026) for Experienced Engineers 24 minutes - FPGA Interview Questions, \u0026 **Answers**, (2026) | 25 Advanced Questions for Experienced Engineers This video covers the Top 25 ... 97ba4acbee Q17: When would you choose high-level synthesis over handwritten RTL? 97ba4acbee Question 14: Explain BRAM and distributed RAM. 97ba4acbee Interview Question FPGA Lab - Interview Question FPGA Lab 4 minutes, 44 seconds - SKEE3742 Specialized lab (**FPGA**, Lab) **Interview questions**, for Group 7 member Sow Ming Han (A17KE0267) 97ba4acbee What happens during Place \u0026 Route? 97ba4acbee Q2: What are LUTs, flip-flops, DSP slices, and block RAMs, and how do they work together? 97ba4acbee Playback 97ba4acbee FPGA Interview Questions Part 1 - FPGA Interview Questions Part 1 13 minutes, 13 seconds - In this video, most commonly asked **interview questions**, are discussed with a good amount of explanation as well. We also have a ... 97ba4acbee Question 3: How does routing work inside an FPGA? 97ba4acbee Q13: What verification strategy would you use for a complex FPGA module? 97ba4acbee Question 23: What is STA (Static Timing Analysis)? 97ba4acbee Tell Me About Yourself | Best Answer (from former CEO) - Tell Me About Yourself | Best Answer (from former CEO) 5 minutes, 15 seconds - In this video, I give the best **answer**, to the job **interview question**, \"tell me about yourself\". This is the best way I've ever seen to ... 97ba4acbee General 97ba4acbee What is a PLL? 97ba4acbee Q7: What reset strategy would you use for a multi-clock FPGA design? 97ba4acbee Question 1: What is the difference between FPGA, CPLD, and ASIC? 97ba4acbee Q1 Write a RTL 97ba4acbee Q1: How does an FPGA differ from a CPU or GPU, and when would you choose one? 97ba4acbee Q7 How many multiplexers are required for implementation of 16x21 97ba4acbee Intro 97ba4acbee What is a SERDES transceiver and where might one be used? 97ba4acbee Question 6: Can you explain metastability in flip-flops? 97ba4acbee Q6: How do you safely transfer signals and data between asynchronous clock domains? 97ba4acbee Question 10: What is a state machine? Explain Mealy vs Moore. 97ba4acbee What is a Black RAM? 97ba4acbee Introduction. 97ba4acbee